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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/069,054	04/28/98	CHAN K	ACT-233

LM02/1221

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EXAMINER	
THOMPSON, A	
ART UNIT	**PAPER NUMBER**
2768	9

DATE MAILED: 12/21/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/069,054	Richard CHAN et al.
Examiner	**Group Art Unit**
A.M. Thompson	2768

☒ Responsive to communication(s) filed on *Apr 29, 1998*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-39* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-39* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *3*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

This application, serial number 09/069,054, has been examined. Claims 1-39 are pending.

Drawings

1. Figures 1A-1F, 2 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated, as also conceded by applicant's specification, page 2, line 12 to page 5, line 1. See MPEP § 608.02(g).

2. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect(s) can be deferred until the application is allowed by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

Rejection of Claims 1-3, 7-9, 11-19

4. Claims 1-3, 7-9 and 11-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Tavana et al., U.S. Patent 5,825,202 (hereinafter "Tavana"). Tavana discloses an integrated circuit with field programmable and application specific logic areas and the interconnections used.

Pursuant to Claim 1 which recites "[a]n interface architecture in an integrated circuit": Tavana, Figs. 3-5 discloses interface architecture that is either mask-defined or FPGA programmable; comprising an FPGA portion of said integrated circuit having logic blocks . . . and interconnect conductors for programmable connections: Tavana, col. 2, ll. 4-9; col. 5, ll. 31-54;

an ASIC portion having mask programmed logic circuits and interconnect conductors: Tavana discloses a mask-defined ASLA, col. 5, ll. 55-64;

masked programmed dedicated interface tracks connected logic blocks in the FPGA and mask programmed interconnect conductors in the ASIC portion: Tavana discloses mask-defined routing for interconnecting FPGA and ASLA.

Pursuant to Claim 2, wherein the interconnect conductors in the FPGA portion include local routing resources: Tavana discloses that local routing resources are included through the use of switch matrices, col. 5, ll. 31-54; also see Fig. 3.

Pursuant to Claim 3, wherein interface buffers are disposes in series with said dedicated interface tracks between FPGA portion and ASIC portion: Tavana discloses the option of interconnections using buffers, col. 6, ll. 34-64.

Pursuant to Claim 7, which further includes an FPGA-ASIC routing channel: Tavana, Fig. 2, col. 5, ll. 13-21.

Pursuant to Fig. 8, wherein the FPGA-ASIC routing channel is mask-programmable: See Tavana, Figs. 3-5 where the routing channel is field configurable and mask programmable; col. 6, ll. 7-27; col. 7, ll. 6-13.

Pursuant to Claim 9, wherein the FPGA-ASIC routing channel is field-programmable: See Tavana, Figs. 3-5 where the routing channel is field configurable and mask programmable; col. 6, ll. 7-27; col. 7, ll. 6-13.

Pursuant to Claim 11 which further includes a plurality of IO modules arranged on the perimeter of the IC: Tavana, Fig. 2, illustrates this limitation; also see col. 4, line 62 to col. 5, line 12.

Pursuant to Claim 12 wherein one or more of said IO modules are connected to said FPGA portion: Tavana, Fig. 2; col. 4, line 62 to col. 5, line 2;

Pursuant to Claim 13 wherein one or more of said IO modules are connected to said ASIC portion: Tavana, Fig. 2; col. 4, line 62 to col. 5, line 2;

Pursuant to Claim 14, which further includes a plurality of IO modules arranged on the perimeter of the IC: This claim possesses the same limitations as Claim 11 and is likewise rejected

for the same reasons: Tavana, Fig. 2, illustrates this limitation; also see col. 4, line 62 to col. 5, line 12.

Pursuant to Claim 15, wherein one or more of said IO modules are connected to said FPGA-ASIC routing channel: Tavana, Figs. 4, 5 illustrates this limitation; also see col. 6, ll. 18-64.

Pursuant to Claim 16, wherein the ASIC portion is adjacent to one side of said FPGA portion: This limitation is illustrated by Tavana, Fig. 2.

Pursuant to Claim 17, wherein the ASIC portion is adjacent to two sides of said FPGA portion: This limitation is inherent to the Tavana invention. One skilled in the art would readily exercise their design prerogative and modify the design architecture so that the ASIC portion is adjacent to two sides of the FPGA portion to facilitate a routing, timing or some other design optimization.

Pursuant to Claim 18, wherein the ASIC portion is adjacent to three sides of said FPGA portion: One skilled in the art would readily exercise their design prerogative and modify the design architecture so that the ASIC portion is adjacent to three sides of the FPGA portion to facilitate a routing, timing or some other design optimization.

Pursuant to Claim 19, wherein the ASIC portion is adjacent to four sides of said FPGA portion: One skilled in the art would readily exercise their design prerogative and modify the design architecture so that the ASIC portion is adjacent to four sides of the FPGA portion to facilitate a routing, timing or some other design optimization.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of Claims 4-6

6. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana as applied to claim 1 above, and further in view of Bertolet et al., U.S. Patent 5,671,432 (hereinafter "Bertolet"). Tavana does not disclose the specific logic used for the discloses programmable I/O blocks. Bertolet discloses a programmable array having programmable logic cells, a programmable interconnect network and a programmable I/O system. Bertolet teaches an advanced I/O system capable of handling high logic densities peculiar to FPGA. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify the teaching of Tavana with Bertolet to provide advanced I/O circuitry for Tavana's dense combined FPGA/ASLA integrated circuit.

Pursuant to Claim 4, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b;

an output buffer, said output buffer connected to said input buffer: Fig. 4, 58a, 58b;

three multiplexors, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, and 52b, 54b, 56b;

a configurable register, said configurable register connected to each of said muxes: Bertolet, Fig. 6 details the muxes illustrated in Fig. 4. Bertolet, Fig. 6 shows memory elements connected to each mux. Bertolet further teaches that the memory contains user programming information which is the same as configuration information, col. 8, ll. 2-16.

Pursuant to Claim 5, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b;

an output buffer, said output buffer connected to said input buffer: Fig. 4, 58a, 58b;

three multiplexors, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, and 52b, 54b, 56b;

a memory store, said memory store connected to each of said muxes: Bertolet, Fig. 6 details the muxes illustrated in Fig. 4. Bertolet, Fig. 6 shows memory elements connected to each mux; also see Bertolet, col. 8, ll. 2-16.

Pursuant to Claim 6, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b;

an output buffer, said output buffer connected to said input buffer: Fig. 4, 58a, 58b;

three multiplexors, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, and 52b, 54b, 56b;

programmable elements, said programmable elements connected to each of said muxes: Bertolet, Fig. 6 details the muxes illustrated in Fig. 4. Bertolet, Fig. 6, shows memory elements connected to each mux; also see Bertolet, col. 8, ll. 2-16 which teaches that the memory contains user *programming* information.

Rejection of Claim 10

7. Claims 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana as applied to claim 1 above, and further in view of Sharma et al., U.S. Patent 5,878,051 (hereinafter "Sharma"). Tavana does not explicitly teach the inclusion of JTAG buffers between the FPGA and the ASIC logic portions. Sharma discloses an FPGA which is reconfigured during a test mode to perform testing of an ASIC or other IC component, col. 2, ll. 18-61. It would have been obvious to one of ordinary skill in the art to modify the teaching of Tavana with Sharma and use the IEEE JTAG standard to provide interface ports between the ASIC and the FPGA to enable testing of the FPGA-ASIC assemblage.

Pursuant to Claim 10 wherein there are JTAG buffers arranged between said dedicated interface tracks and ASIC portions: Sharma, Fig. 2; col. 5, ll. 8-56; see also col. 8, ll. 4-65.

8. Claims 10 is also rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana as applied to Claim 1 above and further in view of Bertolet and Bocchino, U.S. Patent 5,869,979. Tavana does not specifically disclose an I/O interface that conforms with the JTAG standard. Bocchino teaches a technique for configuring the outputs and I/Os of a programmable integrated circuit. Bocchino discloses the IO circuit configuration necessary for conformance with the JTAG standard, Bocchino, Fig. 5; col. 9, line 40 to col. 11, line 53. The IO circuit shown in Bocchino Fig. 5 and described in the Bocchino specification is similar to the IO circuitry shown in Bertolet, Figs. 3-5. The Bertolet I/O interface structurally conforms to the JTAG standard, otherwise known as IEEE 1149.1. It would certainly have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Tavana with the teaching of Bocchino and Bertolet to enable a testing interface that additionally conforms to the IEEE 1149.1 standard.

Rejection of Claims 16-19

9. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana as applied to claim 1 above, and further in view of Applicant's admitted prior art.

Pursuant to Claim 16, wherein said ASIC portion is adjacent to one side of said FPGA portion: Applicant's Prior art, Figs. 1A, 1B.

Pursuant to Claim 17, wherein said ASIC portion is adjacent to two sides of said FPGA portion: Applicant's prior art, Figs. 1C, 1D.

Pursuant to Claim 18, wherein said ASIC portion is adjacent to three sides of said FPGA portion: Applicant's prior art, Figs. 1C, 1D (including the side between the I/O and the FPGA and ASIC.

Pursuant to Claim 19, wherein said ASIC portion is adjacent to four sides of said FPGA portion: Applicant's prior art, Figs. 1E, 1F.

Rejection of Claim 20

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana as applied to claim 1 above, and further in view of the Aggarwal et al. paper (hereinafter the "Aggarwal paper") and Rush, U.S. Patent 5,742,181. Tavana does not teach hierarchical design structures. The Aggarwal paper discloses routing architectures for hierarchical Field Programmable Gate Arrays (FPGAs). Rush discloses FPGAs with hierarchical interconnect structures. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Tavana with the Aggarwal paper and Rush and implement a hierarchical FPGA having the advantages of lower density, increased routing efficiency.

Pursuant to Claim 20, wherein the FPGA portion has a hierarchical design: The Aggarwal paper teaches FPGA hierarchical designs, pp. 475-477. Rush teaches FPGAs or generally programmable atomic logic elements with a hierarchical interconnect structure, col. 4, line 10 to col. 13, line 8.

Rejection of Claims 21-23, 27-29 and 31-36

11. Claims 21-23, 27-29, 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana in view of the Aggarwal paper and Rush. Tavana discloses an integrated circuit with field programmable and application specific logic areas (ASLA) and the interconnections used. Tavana does not teach hierarchical design structures. The Aggarwal paper discloses routing architectures for hierarchical Field Programmable Gate Arrays (FPGAs). Rush discloses FPGAs with hierarchical interconnect structures. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Tavana with the Aggarwal paper and Rush and implement a hierarchical FPGA having the advantages of lower density and increased routing efficiency.

Pursuant to Claim 21 which recites "[a]n interface architecture in an integrated circuit": Tavana, Figs. 3-5 discloses interface architecture that is either mask-defined or FPGA programmable; comprising

"an FPGA portion of said integrated circuit having a plurality of levels . . .": The Aggarwal paper teaches FPGA hierarchical (equivalent in meaning to "plurality of levels") designs, pp. 475-477. Rush teaches FPGAs or generally programmable atomic logic elements with a hierarchical interconnect structure, col. 4, line 10 to col. 13, line 8.

an ASIC portion having mask programmed logic circuits and interconnect conductors: Tavana discloses a mask-defined ASLA, col. 5, ll. 55-64;

masked programmed dedicated interface tracks connected between logic blocks in the FPGA and mask programmed interconnect conductors in the ASIC portion: Tavana discloses mask-

defined routing for interconnecting FPGA and ASLA.

Pursuant to Claim 22, wherein the interconnect conductors in the FPGA portion include local routing resources: Tavana discloses that local routing resources are included through the use of switch matrices, col. 5, ll. 31-54; also see Fig. 3.

Pursuant to Claim 23, wherein interface buffers are disposes in series with said dedicated interface tracks between FPGA portion and ASIC portion: Tavana discloses the option of interconnections using buffers, col. 6, ll. 34-64.

Pursuant to Claim 27, which further includes an FPGA-ASIC routing channel: Tavana, Fig. 2, col. 5, ll. 13-21.

Pursuant to Claim 28, wherein the FPGA-ASIC routing channel is mask-programmable: See Tavana, Figs. 3-5 where the routing channel is field configurable and mask programmable; col. 6, ll. 7-27; col. 7, ll. 6-13.

Pursuant to Claim 29, wherein the FPGA-ASIC routing channel is field-programmable: See Tavana, Figs. 3-5 where the routing channel is field configurable and mask programmable; col. 6, ll. 7-27; col. 7, ll. 6-13.

Pursuant to Claim 31 which further includes a plurality of IO modules arranged on the perimeter of the IC: Tavana, Fig. 2, illustrates this limitation; also see col. 4, line 62 to col. 5, line 12.

Pursuant to Claim 32 wherein one or more of said IO modules are connected to said FPGA portion: Tavana, Fig. 2; col. 4, line 62 to col. 5, line 2;

Pursuant to Claim 33 wherein one or more of said IO modules are connected to said ASIC portion: Tavana, Fig. 2; col. 4, line 62 to col. 5, line 2.

Pursuant to Claim 34, which further includes a plurality of IO modules arranged on the perimeter of the IC: This claim possesses the same limitations as Claim 11 and is likewise rejected for the same reasons: Tavana, Fig. 2, illustrates this limitation; also see col. 4, line 62 to col. 5, line 12.

Pursuant to Claim 35, wherein one or more of said IO modules are connected to said FPGA-ASIC routing channel: Tavana, Figs. 4, 5 illustrates this limitation; also see col. 6, ll. 18-64.

Pursuant to Claim 36 wherein the ASIC portion is adjacent to one side of said FPGA portion: This limitation is illustrated by Tavana, Fig. 2.

Rejection of Claims 24-26

12. Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana in view of the Aggarwal paper and Rush as applied to claim 21 above, and further in view of Bertolet et al., U.S. Patent 5,671,432 (hereinafter "Bertolet"). Bertolet discloses a programmable array having programmable logic cells, a programmable interconnect network and a programmable I/O system. Tavana does not disclose the specific logic used for the discloses programmable I/O blocks. Bertolet discloses a programmable array having programmable logic cells, a programmable interconnect network and a programmable I/O system. Bertolet teaches an advanced I/O system capable of handling high logic densities peculiar to FPGA. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify the teaching of Tavana with Bertolet to provide advanced I/O circuitry for Tavana's dense combined FPGA/ASLA integrated circuit.

Pursuant to Claim 24, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b;

an output buffer, said output buffer connected to said input buffer: Fig. 4, 58a, 58b;

three multiplexors, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, and 52b, 54b, 56b;

a configurable register, said configurable register connected to each of said muxes: Bertolet, Fig. 6 details the muxes illustrated in Fig. 4. Bertolet, Fig. 6 shows memory elements connected to

each mux. Bertolet further teaches that the memory contains user programming information which is the same as configuration information, col. 8, ll. 2-16.

Pursuant to Claim 25, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b;

an output buffer, said output buffer connected to said input buffer: Fig. 4, 58a, 58b;

three multiplexors, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, and 52b, 54b, 56b;

a memory store, said memory store connected to each of said muxes: Bertolet, Fig. 6 details the muxes illustrated in Fig. 4. Bertolet, Fig. 6 shows memory elements connected to each mux; also see Bertolet, col. 8, ll. 2-16.

Pursuant to Claim 26, wherein the interface architecture includes an input buffer: Fig. 4, 60a and 60b;

an output buffer, said output buffer connected to said input buffer: Fig. 4, 58a, 58b;

three multiplexors, two of said muxes connected to said output buffer and one of said muxes connected to said input buffer: Fig. 4, 52a, 54a, 56a, and 52b, 54b, 56b;

programmable elements, said programmable elements connected to each of said muxes: Bertolet, Fig. 6 details the muxes illustrated in Fig. 4. Bertolet, Fig. 6, shows memory elements

connected to each mux; also see Bertolet, col. 8, ll. 2-16 which teaches that the memory contains user *programming* information.

Rejection of Claim 30

13. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana in view of the Aggarwal paper and Rush as applied to claim 21 above, and further in view of Sharma et al., U.S. Patent 5,878,051 (hereinafter "Sharma"). Tavana does not explicitly teach the inclusion of JTAG buffers between the FPGA and the ASIC logic portions. Sharma discloses an FPGA which is reconfigured during a test mode to perform testing of an ASIC or other IC component, col. 2, ll. 18-61. It would have been obvious to one of ordinary skill in the art to modify the teaching of Tavana with Sharma and use the IEEE JTAG standard to provide interface ports between the ASIC and the FPGA to enable testing of the FPGA-ASIC assemblage.

Pursuant to Claim 30 wherein there are JTAG buffers arranged between said dedicated interface tracks and ASIC portions: Sharma, Fig. 2; col. 5, ll. 8-56; see also col. 8, ll. 4-65.

14. Claim 30 is also rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana in view of the Aggarwal paper and Rush as applied to Claim 21 above and further in view of Bertolet and Bocchino, U.S. Patent 5,869,979. Bocchino teaches a technique for configuring the outputs and I/Os of a programmable integrated circuit. Bocchino discloses the IO circuit configuration necessary for conformance with the JTAG standard, Bocchino, Fig. 5; col. 9, line 40 to col. 11, line 53. The IO circuit shown in Bocchino Fig. 5 and described in the Bocchino specification is similar to the IO

circuitry shown in Bertolet, Figs. 3-5. The Bertolet I/O interface structurally conforms to the JTAG standard, otherwise known as IEEE 1149.1. It would certainly have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Tavana with the teaching of Bocchino and Bertolet to enable a testing interface that additionally conforms to the IEEE standard.

Rejection of Claims 36-39

15. Claims 36-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana in view of the Aggarwal paper and Rush as applied to claim 21 above, and further in view of Applicant's admitted prior art.

Pursuant to Claim 36, wherein said ASIC portion is adjacent to one side of said FPGA portion: Applicant's Prior art, Figs. 1A, 1B.

Pursuant to Claim 37, wherein said ASIC portion is adjacent to two sides of said FPGA portion: Applicant's prior art, Figs. 1C, 1D.

Pursuant to Claim 38, wherein said ASIC portion is adjacent to three sides of said FPGA portion: Applicant's prior art, Figs. 1C, 1D (including the side between the I/O and the FPGA and ASIC.

Pursuant to Claim 39, wherein said ASIC portion is adjacent to four sides of said FPGA portion: Applicant's prior art, Figs. 1E, 1F.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

▹Butts et al., U.S. Patent 5,452,231, discloses a hierarchically connected reconfigurable logic assembly.

▹ Kean, U.S. Patent 5,469,003, discloses a hierarchically connectable configurable cellular array.

▹ New, U.S. Patent 5,874,834, discloses a field programmable gate array with distributed gate-array functionality.

▹ McGowan, U.S. Patent 5,959,466, discloses a field-programmable gate array with mask programmed input and output buffers.

▹ Furtek et al, U.S. Patent 5,894,565, discloses a field programmable gate array with distributed RAM and increased cell utilization.

▹Baxter et al., U.S. Patent 5,991,908, discloses a boundary scan chain with dedicated programmable routing.

▹ Lee et al., U.S. Patent 5,883,850, discloses a programmable logic array integrated circuit.

▹ Ashby et al., U.S. Patent 5,347,181, discloses an interface control logic for embedding a microprocessor in a gate array.

▹ Agarwala, U.S. Patent 5,338,983, discloses an Application Specific Exclusive-Or Based Architecture for FPGAs.

▹Ashby et al, U.S. Patent 5,304,860, discloses a method for powering down a microprocessor embedded within a gate array.

▹ Chen et al., U.S. Patent 5,835,751, discloses a structure and method for providing a reconfigurable emulation circuit.

▹ Trimberger et al., U.S. Patent 5,594,367, discloses an output multiplexer within input/output circuit for time multiplexing and high speed logic.

▹ El Gamal et al., U.S. Patent 4,873,459, discloses a user-programmable interconnect architecture.

▹Chene et al., U.S. patent 5,224,056, discloses a modified partitioning method for placement of a circuit design into a programmable integrated circuit device.

▹ El Gamal et al., U.S. Patent 4,758,745, discloses a user programmable integrated circuit interconnect architecture and test method.

▹ L.R. Ashby, Interface Techniques for Embedding Custom Mega Cells in a Gate Array, teaches a method to allow semiconductor companies to reuse existing custom circuit designs in a cell based or gate array environment.

▹M. Karjalainen et al., Block Diagram Compilation and Graphical Editing of DSP Algorithms in the QuickSig System, teaches a method that uses a block diagram compiler and an interactive graphical editor in DSP software development.

▷A. El Gamal et al., An Architecture for Electrically Configurable Gate Arrays, teaches a novel architecture that combines the flexibility of mask-programmable arrays with the convenience of field programmability.

▷ M. Agarwala et al., An Architecture for a DSP Field-Programmable Gate Array, discloses an application specific architecture for field-programmable gate arrays.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Paul Lintz, can be reached on (703) 305-3832. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-9051.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900 or the Customer Service Center whose telephone number is (703)306-5631.

18. Responses to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 305-9051, (for formal communications intended for entry)

(703) 305-0040 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

AMT
DECEMBER 17, 1999

Paul R. Lintz
Primary Examiner